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Finite State Machines In Hardware: Theory And Design (with VHDL And SystemVerilog) (MIT Press)



Synopsis

Modern, complex digital systems invariably include hardware-implemented finite state machines. The correct design of such parts is crucial for attaining proper system performance. This book offers detailed, comprehensive coverage of the theory and design for any category of hardware-implemented finite state machines. It describes crucial design problems that lead to incorrect or far from optimal implementation and provides examples of finite state machines developed in both VHDL and SystemVerilog (the successor of Verilog) hardware description languages. Important features include: extensive review of design practices for sequential digital circuits; a new division of all state machines into three hardware-based categories, encompassing all possible situations, with numerous practical examples provided in all three categories; the presentation of complete designs, with detailed VHDL and SystemVerilog codes, comments, and simulation results, all tested in FPGA devices; and exercise examples, all of which can be synthesized, simulated, and physically implemented in FPGA boards. Additional material is available on the book's Website. Designing a state machine in hardware is more complex than designing it in software. Although interest in hardware for finite state machines has grown dramatically in recent years, there is no comprehensive treatment of the subject. This book offers the most detailed coverage of finite state machines available. It will be essential for industrial designers of digital systems and for students of electrical engineering and computer science.

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Customer Reviews

This book by Dr. Pedroni is a first of a kind comprehensive treatment of FSM hardware design covering examples in VHDL and SystemVerilog. It covers important topics of FSM hardware implementation normally known to experience designers such as Hierarchical FSM's and Timed FSM. Another aspect is it points out subtle mistakes that designers tend to make during design and coding. Although there are good number of examples in the book, but I would have liked to see some atleast 3-4 examples with bigger and more complicated controller designs (network controllers for example or other state of the art controllers). Another missing topic is verification and testbench design for FSM's. I would recommend this book for designers with few years of experience and looking to designing complicated controllers. For experienced designers, this book may not be much relevant as majority of content will be familiar to them.

Book is brand new. Regarding the content, I was disappointed for not seeing more System-Verilog examples, which were mostly been translated from VHDL.

This book is a comprehensive one full of usefull and practical technical details and applications. Nice and good work and Thanks!

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